Exhibit 2

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Paper 42
Date: October 17, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00711
Patent 10,860,506 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00205 and have been joined as petitioners in this proceeding.

I. INTRODUCTION

In this *inter partes* review, Samsung Electronics Co., Ltd. ("Samsung"), Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 1–20 of U.S. Patent No. 10,860,506 B2 (Ex. 1001, "the '506 patent"), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–20 of the '506 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Samsung filed a Petition (Paper 1, "Pet.") challenging claims 1–20 of the '506 patent on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)[2]	Hiraishi,[3] Butt[4]
3, 5, 12, 16	103(a)	Hiraishi, Butt, Ellsberry[5]

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. For this proceeding, Petitioner assumes that the '506 patent has an effective priority date before this date (Pet. 2) and applies the pre-AIA version of § 103.
[3] Ex. 1005, US 2010/0312956 A1, published Dec. 9, 2010.
[4] Ex. 1029, US 2007/0008791 A1, published Jan. 11, 2007.
[5] Ex. 1007, US 2006/0277355 A1, published Dec. 7, 2006.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
8–10, 19, 20	103(a)	Hiraishi, Butt, Kim[6]
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt, Tokuhiro[7]
3, 5, 12, 16	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Tokuhiro, Kim

Pet. 1–2. Patent Owner filed a Preliminary Response. Paper 7. As authorized (Paper 9), Samsung filed a reply (Paper 12), and Patent Owner filed a sur-reply (Paper 13). Trial was instituted on the asserted grounds of unpatentability. Paper 11 ("Inst. Dec."), 34.

After institution, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00205, and we joined these entities as petitioners in this proceeding. Paper 26.

During the trial, Patent Owner filed a Response (Paper 23, "PO Resp."), Petitioner filed a Reply (Paper 30, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 35, "PO Sur-reply").

An oral hearing was held on July 20, 2023, a transcript of which appears in the record. Paper 41 ("Tr.").

Petitioner relies on testimony from Dr. Robert Wedig. Ex. 1003. Patent Owner relies on testimony from Dr. William Henry Mangione-Smith. Ex. 2006.[8] The parties have entered in the record transcripts for depositions of these declarants. Exs. 1046 (Mangione-Smith Deposition), 2008 (Wedig Deposition), 1055 (Wedig Deposition Errata).

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[6] Ex. 1008, US 6,184,701 B1, issued Feb. 6, 2001.
[7] Ex. 1006, US 8,020,022 B2, issued Sept. 13, 2011.
[8] Before institution, Patent Owner submitted testimony from Dr. Sunil P. Khatri. Ex. 2005. Patent Owner does not cite this testimony in its post-institution briefing. *See* PO Resp., PO Sur-reply.

B. Real Parties in Interest

Petitioner identifies the following as real parties in interest: Samsung, Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Pet. xxiii; IPR2023-00205, Paper 3 at 1.

Patent Owner identifies itself as the real party in interest. Paper 5 at 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters. Pet. xxiii; Paper 3 at 1; IPR2023-00205, Paper 3 at 1–2.

D. The '506 Patent and Illustrative Claim

The '506 patent is titled "Memory Module with Timing-Controlled Data Buffering" and discloses adjusting the timing of certain signals in memory based on previous operations. Ex. 1001, codes (54), (57). Claims 1 and 14 are the independent claims of the '506 patent. Claim 1 is reproduced below.

> 1. A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
>
> a module board having edge connections to be coupled to respective signal lines in the memory bus;
>
> a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
>
> memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data

and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe;

data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sample the first section of the read data using the first delayed read strobe; and

transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

II. ANALYSIS

A. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art;

(2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.[9] *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art "would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field," and would have had knowledge of various standards for memory, such as Joint Electron Devices Engineering Council (JEDEC) standards, and circuitry used in memories. Pet. 2–3 (citing Ex. 1003 ¶ 37). Patent Owner asserts that it is "applying the level of ordinary skill in the art proposed by Petitioner." PO Resp. 11.

We adopt Petitioner's uncontested level of ordinary skill with the exception of the phrase "at least," which introduces vagueness as to the amount of experience.

C. Claim Construction

We agree with the parties that we need not construe expressly any claim terms to decide the issues before us. *See* Pet. 9; PO Resp. 11; *see also Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy,

[9] The parties do not present arguments related to objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over Hiraishi and Butt (Claims 1, 2, 4, 6, 7, 11, 13–15, 17, 18)

Petitioner asserts that claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 would have been obvious over the combined teachings of Hiraishi and Butt. Pet. 20–68. Patent Owner opposes. PO Resp. 22–48; PO Sur-reply 1–13.

1. Overview of the Prior Art

Hiraishi, titled "Load Reduced Memory Module," discloses a memory system having a plurality of memory chips connected to data buffers. Ex. 1005, codes (54), (57), Fig. 1. Hiraishi discloses that the data buffers have circuitry that delays data strobe signals (DQS). Ex. 1005 ¶ 91.

Butt, titled "DQS Strobe Centering (Data Eye Training) Method," discloses "read training" that is used "to establish optimum DQS strobe settings" and to "shift the DQS strobe to be optimally positioned relative to DQ (valid read data)." Ex. 1029, code (54), ¶ 33. Butt discloses using the read training process in a strobe-centering technique, which involves "adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window." Ex. 1029 ¶ 35.

We discuss additional pertinent details of Hiraishi and Butt in our analysis below.

2. Claim 1

a) Preamble and Undisputed Limitations

The preamble of claim 1 recites a "memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines

and a data bus." Petitioner identifies Hiraishi's memory module 100 as the recited "memory module," memory control hub (MCH 12) as the recited "memory controller," and bus 23 with data lines L0 as the recited "data bus." Pet. 21 (citing Ex. 1005 ¶¶ 65, 69, Figs. 1–3; Ex. 1003 ¶¶ 101–102). Petitioner argues that Hiraishi's memory module 100 connects to MCH 12 by a memory bus 23 and that bus 23 includes a set of control/address signal lines. Pet. 22–23 (citing Ex. 1005 ¶¶ 47, 49, 60, 69, 102–103, 107, Figs. 1, 3, 7; Ex. 1003 ¶¶ 102–103).

Claim 1 recites that the memory module comprises "a module board having edge connections to be coupled to respective signal lines in the memory bus." Petitioner identifies Hiraishi's module substrate 110 as the recited "module board" and command/address/control connectors 130 and data connectors 120 as the recited "edge connections." Pet. 23 (citing Ex. 1005 ¶¶ 45, 47–49, Fig. 1; Ex. 1003 ¶¶ 104–107).

Claim 1 recites that the memory module comprises "a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals." Petitioner identifies Hiraishi's command/address/control register buffer 400 as the recited "module control device on the module board." Pet. 24–25 (citing Ex. 1005 ¶ 59, Fig. 1; Ex. 1003 ¶¶ 108–109). Petitioner argues Hiraishi's register buffer 400 is configurable to receive C/A signals corresponding to a read operation through command/address/control connectors 130 and line L3 and to output C/A signals and control signals, such as the DRC and Clock-Post signal, on lines L4 and L5. Pet. 25 (citing Ex. 1005 ¶¶ 18–19, 47, 60, 97, 99, Figs. 1, 6, 7; Ex. 1003 ¶ 110).

Claim 1 recites that the memory module comprises "memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals." Petitioner argues that Hiraishi teaches memory devices, depicted in Figure 1 as 200-0 to 200-35, arranged in four different ranks on module board 110 and coupled to register buffer 400 by data line L5. Pet. 28–29 (citing Ex. 1005 ¶¶ 45, 50–52, 107, Figs. 1, 7; Ex. 1003 ¶¶ 114–116).

Claim 1 recites

> wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe.

Petitioner argues that Hiraishi's memory devices 200 are situated in ranks and correspond to respective sets of data/strobe signal lines such as line L0 depicted in Figure 7 and are connected to data register buffers. Pet. 30 (citing Ex. 1005 ¶¶ 51–54, 56, 76, 79–80, 103, 120–129, Figs. 1, 4, 7; Ex. 1003 ¶ 119). Petitioner argues that, consistent with the JEDEC standard, read commands include a chip select signal that commands all memory devices in the selected rank to perform the commands together. Pet. 30–31 (citing Ex. 1021, 319, 413; Ex. 1020, 13, 22, 34 n.1; Ex. 1018, 4.20.4-6, 4.20.4-10–4.20.4-16; Ex. 1003 ¶¶ 120–121).

Claim 1 recites that the memory module comprises

> data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device.

Petitioner argues that Hiraishi's data register buffers 300 are positioned between the set of memory devices 200 and the connectors 120 connecting to the data line L0 and that the data register buffers 300 are coupled to memory devices 200. Pet. 31 (citing Ex. 1003 ¶¶ 122–126). Petitioner argues that data buffer 300 receives module command/address/control line L4 from command/address/control register buffer 400. Pet. 31–33 (citing Ex. 1005, Figs. 1, 5, 7; Ex. 1003 ¶¶ 122–126).

Patent Owner does not dispute Petitioner's contentions for these limitations of claim 1. We find Petitioner's contentions persuasive, and we find that Hiraishi teaches the subject matter of these limitations.

b) Disputed Limitations

Claim 1 recites,

> wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
>
> delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
>
> sample the first section of the read data using the first delayed read strobe; and
>
> transmit the first section of the read data to a first section of the data bus;
>
> wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

Petitioner argues that Hiraishi teaches a first data buffer (data register buffer 300) that is coupled to the first memory device (memory devices 200) and is configurable to perform the recited operations. Pet. 34 (citing Ex. 1005 ¶¶ 45, 55–56, 84, 99, 103, Figs. 1, 7; Ex. 1003 ¶¶ 127–128). Petitioner provides the following annotated version of Hiraishi's Figure 5:

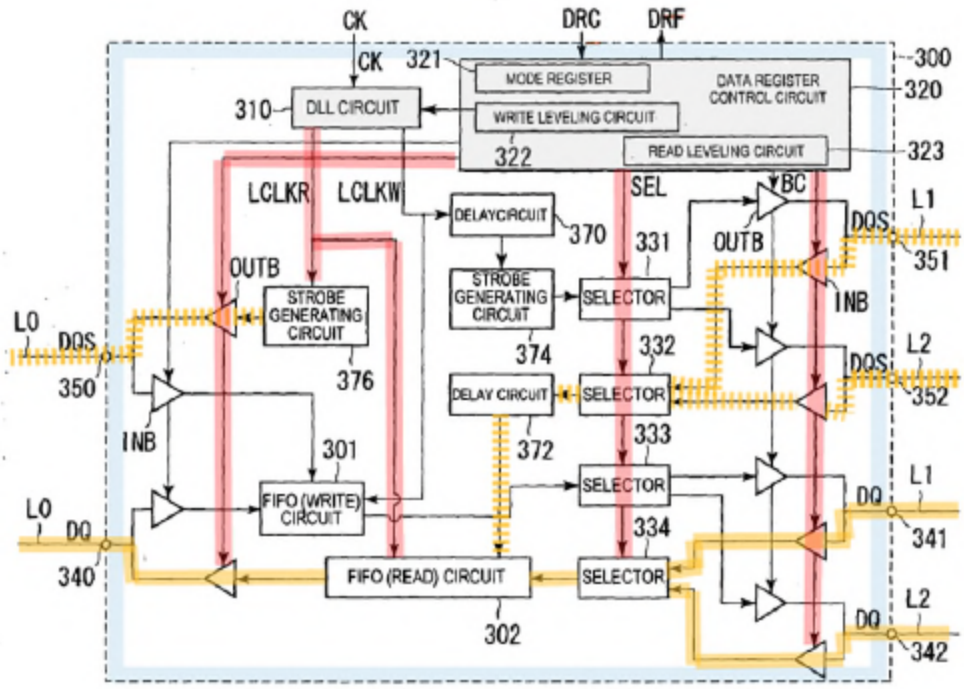

FIG.5

Pet. 36. Hiraishi's Figure 5 is a block diagram of data register buffer 300, including read leveling circuit 323, delay circuit 372, and FIFO (first in first out) read circuit 302. Ex. 1005 ¶¶ 83–84, 90–91. In the annotated figure above, Petitioner uses dashed orange lines to show the paths of read strobes, orange lines to show the paths of read data, and pink lines to show the paths of various control signals. *See* Pet. 35–38.

For the delay operation, Petitioner argues that Hiraishi's data register buffers (300) include delay circuit 372 and can delay the first read strobe (DQS signal at input 351) by about 90 degrees to generate a first delayed read strobe to the FIFO (Read) Circuit 302. Pet. 35–36 (citing Ex. 1005 ¶ 91, Fig. 5; Ex. 1003 ¶¶ 99–100, 129–130). Petitioner argues that, in Hiraishi's data register buffer 300, the read data are sampled when they are latched into FIFO read circuit 302 using the delayed strobe and that the data are then transmitted to the data bus, as depicted in the annotated figure above with an orange line from FIFO read circuit 302 to input/output

terminal 340 and on to data line L0. Pet. 36–37 (citing Ex. 1005 ¶ 91, Fig. 5; Ex. 1003 ¶¶ 131–133), 38–39 (citing Ex. 1005, Figs. 1, 5; Ex. 1003 ¶¶ 134–135).

Claim 1 recites, "wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations." Petitioner argues that Hiraishi's reference to delaying the DQS signal by *about* 90 degrees is to allow for fine timing adjustments to the DQS signals by read leveling circuit 323 through a read leveling operation. Pet. 40 (citing Ex. 1005 ¶¶ 90–91, 140, Fig. 13; Ex. 1003 ¶¶ 137–138). Petitioner argues that read leveling in Hiraishi includes performing a read operation, which means that the amount of delay applied to the strobe signal DQS by delay circuit 372 would be based at least on signals received by the data buffer 300 during read leveling. Pet. 42–43 (citing Ex. 1005 ¶¶ 28, 140; Ex. 1003 ¶¶ 142–143).

Alternatively, with respect to the combination of Hiraishi and Butt, Petitioner argues that Butt discloses circuit 104 that can delay read strobe signal DQS that is used to read data signal DQ. Pet. 44 (citing Ex. 1029 ¶¶ 17–18, Fig. 3A; Ex. 1003 ¶ 145). Petitioner argues that Butt describes a method of "read training" that can establish optimum DQS settings by adjusting a delay of the read data strobe signal DQS. Pet. 44–45 (citing Ex. 1029 ¶¶ 33, 35, Fig. 3A; Ex. 1003 ¶¶ 145–147). Petitioner contends that the optimum DQS settings established during read training are then used during later read operations, which a person of ordinary skill in the art would understand as delaying the data strobe signal by a predetermined amount based on signals received during a previous operation (e.g., the dummy data and strobe signals received during read training). Pet. 47 (citing Ex. 1029 ¶¶ 22, 46, 54, 61, Figs. 5–7; Ex. 1003 ¶¶ 148, 150).

Petitioner argues that it would have been obvious to apply Butt's teachings to Hiraishi to set the delay for Hiraishi's delay circuit 372 by read leveling circuit 323 based on signals received during a prior read leveling process. Pet. 47 (citing Ex. 1003 ¶¶ 149–150). According to Petitioner, "Butt provides the motivation: to 'enable[] a reliable data read operation for high speed applications."[10] Pet. 47 (emphasis omitted, alteration by Petitioner) (quoting Ex. 1029 ¶ 36). Petitioner also argues that a person of ordinary skill would have "had a reasonable expectation of success because the combination would be a simple application of known techniques to improve similar technology in a similar way, and Butt's calibration process 200 would offer the same benefit for Hiraishi's delay circuit 372 as for Butt." Pet. 47–48 (emphasis omitted) (citing Ex. 1003 ¶¶ 149–150).

Patent Owner does not dispute that Hiraishi teaches delaying the read strobe, sampling the read data using the delayed read strobe, and transmitting the read data to the data bus. Rather, Patent Owner disputes whether the combination of Hiraishi and Butt teaches delaying the read strobe by a first predetermined amount that "is determined based at least on signals received by the first data buffer during one or more previous operations," as recited in claim 1. *See* PO Resp. 22–48. For the reasons explained below, we find persuasive Petitioner's contentions based on the combined teachings of Hiraishi and Butt.

Patent Owner argues that Petitioner has not shown that a person of ordinary skill in the art would have had a reasonable expectation of success

[10] Petitioner emphasizes, by underline, each instance of the names of the prior art references in its Petition. Unless otherwise noted, we omit these emphases in our quotations from the Petition.

in achieving the claimed invention (PO Resp. 33–40) or would have been motivated to combine the teachings of Hiraishi and Butt (PO Resp. 41–48).

Turning first to the motivation to combine, as noted above, Petitioner argues that Butt's disclosure that its read training technique "generally enables a reliable data read operation for high speed applications" (Ex. 1029 ¶ 36) provides a reason to combine. Pet. 47. Patent Owner, however, contends that Hiraishi deals with DDR3 technology that is newer than Butt's DDR disclosures and that Hiraishi performs reliably. PO Resp. 41–44. Patent Owner further argues that "Hiraishi's data buffers already receive DQ data that is edge aligned with the DQS" and, therefore, that "the problem to which Butt is directed simply does not exist in Hiraishi." PO Resp. 46–47; *see also* PO Resp. 26–27 (arguing that "the DQ data and DQS strobe received by the data buffer from any given memory device [are] always edge-aligned"). According to Patent Owner, "[t]he DDR3 standard requires [a] DDR3-compliant memory device to provide DQ data and DQS strobes edge-aligned, even defining the maximum permitted DQS-DQ skew," obviating the need for Butt's read training. PO Resp. 48 (citing Ex. 2006 ¶¶ 122–124).

We disagree with Patent Owner's arguments because, as Petitioner points out, the evidence shows that DDR3 devices do not always have edge-aligned data and strobes. *See* Pet. Reply 4. In particular, Patent Owner's declarant Dr. Mangione-Smith testifies that the DDR3 standard allows a 200 picosecond maximum DQS-to-DQ skew, "which is a very tight tolerance considering the speed at which the memory devices are operating." Ex. 2006 ¶¶ 122–125 (citing Ex. 1020, 164). During cross-examination of Dr. Mangione-Smith, Petitioner established that a 200 picosecond tolerance is actually a misalignment of over 28 degrees considering the 2.5

nanosecond (2500 picosecond) clock cycle. Ex. 1046, 163:5–166:18; *see* Pet. Reply 4 (discussing this testimony). Thus, the evidence shows that DDR3 data and strobes are not always edge-aligned.

Patent Owner dismisses this, stating that "Petitioner's argument is tantamount to saying that the JEDEC standard prescribes a tolerance for DQS/DQ skew that causes errors, which runs counter to the entire standard-setting process." PO Sur-reply 3–4. On the contrary, we find that Petitioner's showing underscores that Butt's read training has direct applicability to a memory that may potentially skew by as much as 28 degrees. Butt explains that read training is used "to establish optimum DQS strobe settings" and thereby "enables a reliable data read operation for high speed applications." Ex. 1029 ¶¶ 33, 36; *see* Pet. 44–47 (discussing this disclosure). As the Supreme Court has stated, "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. "This is the so-called 'known-technique' rationale. And if there's a known technique to address a known problem using 'prior art elements according to their established functions,' then there is a motivation to combine." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (citing *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 799–800 (Fed. Cir. 2021)). We find that Butt's read training is such a known technique that would improve Hiraishi's memory based on the benefits identified in Butt and discussed above, i.e., "establish[ing] optimum DQS strobe settings" to enable "reliable data read operation for high speed applications." Ex. 1029 ¶¶ 33, 36.

Patent Owner also argues that "Hiraishi uses an entirely different re-timing operation" to account for flight time differences between memory devices, pointing to Hiraishi's retiming operation that is performed after the data are loaded in FIFO (Read) circuit 302. PO Resp. 45 (citing Ex. 1005 ¶ 130). But Petitioner's obviousness contentions are based on adjusting the timing of strobes before the data are registered in (loaded into) FIFO (Read) circuit 302. *See* Pet. 35–37 (asserting that the delayed read strobe is "the DQS signal supplied to FIFO (Read) circuit 302," which is then used to register the data in FIFO (Read) circuit 302). Thus, Patent Owner is pointing to an entirely different operation. Furthermore, even if Hiraishi discloses some mechanism to cope with misaligned data and strobes, we find that Butt's technique is a "suitable option" in combination with Hiraishi. *See Intel*, 61 F.4th at 1381. Indeed, in such a case, Hiraishi and Butt "address the same problem," and Butt's read training "was a known way to address that problem[, which] is precisely the reason that there's a motivation to combine under *KSR* and [Federal Circuit] precedent." *Intel*, 61 F.4th at 1380. Thus, it is not necessary for Petitioner to "identify what details are allegedly missing from Hiraishi which are being provided by Butt," as asserted by Patent Owner. *See* PO Resp. 44.

Turning second to the issue of reasonable expectation of success, Patent Owner argues that the proposed combination would not work for various reasons. PO Resp. 33–40. For example, Patent Owner argues that "Hiraishi's data register control circuit 320 (which includes the read leveling circuit 323) is neither physically nor functional[ly] connected to the delay circuit 372" and, therefore, that read leveling circuit 323 would not be able to control delay circuit 372 to adjust the strobe timing based on the teachings of Butt. PO Resp. 35–38; *see also* PO Resp. 28–32 (contending that read

leveling circuit 323 does not control delay circuit 372). Patent Owner also focuses on differences between Butt's and Hiraishi's systems, arguing, for example, that Butt's strobe-centering technique requires generating a GATEON signal but that Petitioner has not explained how Hiraishi can generate the GATEON signal. PO Resp. 38 (citing Ex. 1029 ¶ 24).

We disagree with Patent Owner's arguments. As an initial matter, the Federal Circuit has

> consistently held . . . that "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art."

MCM Portfolio LLC v. Hewlett-Packard Co., 812 F.3d 1284, 1294 (Fed. Cir. 2015) (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). Thus, Petitioner is not required to show a physical combination of two systems.

Furthermore, Patent Owner's arguments suggest that Butt's read training teachings are confined to Butt's particular memory implementation. Butt's teachings, however, are not so limited. For example, Figures 5–7 of Butt are flowcharts illustrating the training process and processes for determining maximum and minimum offset delays. Ex. 1029 ¶¶ 12–14, 37, 48, 55. Patent Owner argues that these processes "are 'implemented as computer executable code,' which is executed by a digital processor, such as a conventional general purpose digital computer programmed accordingly." PO Resp. 39 (citing Ex. 1029 ¶¶ 45, 62; Ex. 2006 ¶ 102). According to Patent Owner, "Hiraishi's data register buffer does not and cannot include a computer to carry out Butt's strobe-centering process." PO Resp. 39. Butt,

however, does not require a "computer" to perform the process; rather, Butt discloses the following:

> The functions performed by the flow diagrams of FIG. 5–7 *may be implemented* using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

Ex. 1029 ¶ 62 (emphasis added). In fact, Butt discloses other ways its invention "may also be implemented," including with "application specific integrated circuits (ASICs), application specific standard products (ASSPs), field programmable gate arrays (FPGAs), or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s)." Ex. 1029 ¶ 63; *see* Pet. Reply 14 (noting that Butt's implementation can be via ASIC). Thus, we disagree with Patent Owner's arguments that Butt's read training teachings must be implemented with particular circuitry that Hiraishi lacks. Rather, we find that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Butt's read training techniques with Hiraishi's memory teachings to achieve the claimed invention. This finding is supported by Butt's own disclosure that a person of ordinary skill in the art would have been capable of implementing its read training techniques in various ways, as discussed above. *See* Ex. 1029 ¶¶ 62–63. Butt's disclosures support Dr. Wedig's testimony that "application of the techniques in Butt to set the delay in the delay circuit 372 of Hiraishi, e.g., by the read leveling circuit 323, would be a simple

application of known techniques to improve similar technology." Ex. 1003 ¶ 149.

For the reasons discussed above and based on Petitioner's contentions and evidence, we find that the combination of Hiraishi and Butt teaches "delay[ing] the first read strobe by a first predetermined amount to generate a first delayed read strobe," "wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations," as well as the "sample" and "transmit" operations recited in claim 1. We also find, as discussed above, that a person of ordinary skill in the art would have combined the teachings of Hiraishi and Butt and would have had a reasonable expectation of success in arriving at the claimed invention.

c) Conclusion for Claim 1

We conclude that the subject matter of claim 1 would have been obvious based on the combined teachings of Hiraishi and Butt.

3. Claim 14

Independent claim 14 is a method claim that recites structure similar to the structure of claim 1 and steps that are similar to the operations of claim 1. For claim 14, Petitioner refers to its contentions for similar subject matter in claim 1. Pet. 61–64. One difference is that claim 14 recites "each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks." Petitioner cites Hiraishi's disclosure that each of the data buffers "inputs and outputs 1-byte data," i.e. 8 bits. Pet. 62 (quoting Ex. 1005 ¶ 85).

Patent Owner's arguments for claim 1, which we address above, apply to claim 14 (*see* PO Resp. 32, 65), and Patent Owner does not set forth any additional arguments for claim 14.

For the reasons discussed above and in § II.D.2 for claim 1 and based on Petitioner's persuasive contentions and evidence, we conclude that the subject matter of claim 14 would have been obvious based on the combined teachings of Hiraishi and Butt.

4. Dependent Claims 2, 4, 6, 7, 11, 13, 15, 17, 18

Petitioner contends that dependent claims 2, 4, 6, 7, 11, 13, 15, 17, and 18 are unpatentable as obvious over the combined teachings of Hiraishi and Butt. Pet. 48–61, 64–68. Apart from its arguments as to the independent claims, Patent Owner does not dispute Petitioner's contentions for these claims. *See* PO Resp. Below we summarize Petitioner's contentions and evidence, which we find persuasive.

Claim 2 recites,

> The memory module of claim 1, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:
>
> delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;
>
> sample the second section of the read data using the second delayed read strobe; and
>
> transmit the second section of the read data to a second section of the data bus;
>
> wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.

Claim 15 depends from claim 14 and recites similar subject matter.

Petitioner argues that Hiraishi discloses other memory devices in the same rank connected to different buffers, citing memory device 200-32 connected to buffer 300-8 in Hiarishi's Figure 1. Pet. 48–51 (citing Ex. 1005, Figs. 1, 7; Ex. 1003 ¶¶ 152–155); *see* Pet. 30, 34 (identifying memory device 200-0 as the "first memory device" connected to data buffer 300-0 ("first data buffer")); *see also* Pet. 64 (addressing claim 15). Hiraishi discloses that Figure 1 shows a "4-Rank configuration" in which the memories in a single set (e.g., 200-0 through 200-3) belong to different ranks (Ex. 1005 ¶¶ 51–52), thus supporting Petitioner's contention that memory device 200-32 is in the same rank as memory device 200-0. *See* Pet. 49–50. Petitioner contends that the second buffer, in the proposed combination of Hiraishi and Butt, would operate to delay the second read strobe in the same manner as the first buffer in claim 1, thereby rendering obvious the subject matter of claims 2 and 15. Pet. 51–53 (citing Ex. 1005, Figs. 1, 7; Ex. 1003 ¶¶ 156–162), 65 (referring to claim 2 contentions for claim 15).

Claim 4 recites,

> The memory module of claim 2, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.

Claim 17 depends from claim 15 and recites subject matter similar to claim 4. Claim 6 similarly recites, "The memory module of claim 1, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation."

Petitioner argues that Hiraishi and Butt disclose receiving strobe (DQS) signals during previous operations to perform the read leveling and read training procedures discussed with respect to claim 1. Pet. 53–54 (citing Ex. 1003 ¶¶ 163–166), 54 (referring to claim 4 contentions for claim 6), 65 (referring to claim 4 contentions for claim 17).

Claim 7 recites,

> The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:
>
> receive the module clock signal;
>
> generate a local clock signal having a programmable phase relationship with the module clock signal; and
>
> output the local clock signal;
>
> wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

Petitioner argues that control device 400 in Hiraishi's Figure 7 receives a system clock signal and outputs a module clock signal, which is received by the data buffers. Pet. 54–57 (citing Ex. 1005 ¶¶ 60, 108, Figs. 5–7; Ex. 1003 ¶¶ 168–169). Petitioner argues that the DLL circuit in the data buffer "has the same function as DLL 212 in the memory device, which includes generating local clock signals with a programmable phase relationship relative to the clock signal CK." Pet. 57–58 (citing Ex. 1005 ¶¶ 74, 163). Petitioner cites Hiraishi's disclosure that, when the memory chips do not have DLL circuits, the DLL circuit in the data buffer is used to adjust input/output timing (Ex. 1005 ¶ 200). Pet. 58. Petitioner argues that, in this configuration, the data buffer would output a local clock signal, which the memory device receives and uses to output data and read strobes.

Pet. 58–60 (citing Ex. 1005 ¶ 200; Ex. 1009, 4:5–14, 4:31–41, Figs. 1A, 1B; Ex. 1007, Figs. 10–13; Ex. 1003 ¶¶ 172–174).

Claim 18 depends from claim 14 and recites subject matter similar to claim 7, and Petitioner accounts for the differences between the claims, including claim 18's recitations of "receiving, at the module control device, a system clock signal *concurrently with receiving the input C/A signals*" and "outputting, at the module control device, a module clock signal *concurrently with outputting the module control signal*" (emphases added). Pet. 66–68 (citing Ex. 1005 ¶¶ 19, 60, 98–99, 108, Figs. 6, 7; Ex. 1003 ¶¶ 204–211).

Claim 11 recites, "The memory module of claim 1, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations." Petitioner argues that the combination of Hiraishi and Butt teaches circuitry that determines the predetermined amount of delay, referring to its contentions for claim 1. Pet. 61 (citing Ex. 1003 ¶¶ 176–177).

Claim 13 recites, "The memory module of claim 1, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory." Petitioner cites Hiraishi's disclosures of memory devices that are DRAMs and DDR3 DRAMs. Pet. 61 (citing Ex. 1005 ¶¶ 50, 163, 170; Ex. 1021, 465, 471–72, 476–77; Ex. 1020, 56, 59, 69; Ex. 1003 ¶ 178).

As noted above, Patent Owner does not raise additional arguments for these claims. Petitioner's arguments and evidence, summarized above, are persuasive. Therefore, having considered the full record developed during

the trial, we conclude that claims 2, 4, 6, 7, 11, 13, 15, 17, and 18 are unpatentable as obvious over the combined teachings of Hiraishi and Butt.

E. Obviousness over Hiraishi, Butt, and Ellsberry (Claims 3, 5, 12, 16)

Petitioner asserts that claims 3, 5, 12, and 16 would have been obvious over the combined teachings of Hiraishi, Butt, and Ellsberry. Pet. 68–78. Apart from its arguments as to the independent claims, Patent Owner does not dispute Petitioner's contentions for these claims. *See* PO Resp. Below we summarize Petitioner's contentions and evidence, which we find persuasive.

Claim 3 recites,

> The memory module of claim 2, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:
>
> delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;
>
> sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and
>
> transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;
>
> wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

Claim 16 depends from claim 15 and recites, "wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe,

the method further comprising" steps that correspond to the operations recited in claim 3.

Claim 5 recites,

> The memory module [of] claim 2, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

Claim 12 depends from claim 1 and recites, "wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4."

Petitioner argues that "using either 4-bit or 8-bit wide memory devices on a module was well-known at the time and standardized by JEDEC" and would have been obvious to a person of ordinary skill in the art. Pet. 68–69 (citing Ex. 1005 ¶ 73; Ex. 1020, 1, 3–12; Ex. 1018, 4.20.4-12, -15, -25 to -27; Ex. 1021, 370–71, Table 8.1; Ex. 1003 ¶¶ 212–213). Petitioner also relies on Ellsberry's disclosure of using either 8-bit wide memory devices or pairs of 4-bit wide memory devices. Pet. 69–70 (citing Ex. 1007 ¶¶ 51, 54, Figs. 2, 6, 11; Ex. 1020, 6; Ex. 1003 ¶¶ 214–216). Petitioner argues that a person of ordinary skill in the art "would know that different arrangements of 4-bit wide (i.e., 'x4') memory devices were possible" and that "x4 memory devices can be stacked to conserve space." Pet. 71–72 (citing Ex. 1018, 4.20.4-8, -14, -31; Ex. 1020, 6; Ex. 1003 ¶ 217). Petitioner identifies other configurations involving x4 memory devices and argues that "[e]ach of these physical arrangements was well known and obvious."

Pet. 72–73 (citing Ex. 1007 ¶ 51, Figs. 6, 11; Ex. 1020, 6; Ex. 1018, 4.20.4-8, -9, -15, -21, -35; Ex. 1003 ¶ 217).

Petitioner provides a detailed explanation of how the combination of Hiraishi, Butt, and Ellsberry teaches the limitations of claim 3 using 4-bit memory devices. Pet. 70–77. For claims 5, 12, and 16, Petitioner refers to its contentions for claim 3. Pet. 77–78.

As noted above, Patent Owner does not raise additional arguments for these claims. Petitioner's arguments and evidence, summarized above, are persuasive. In particular, we find persuasive Petitioner's arguments that using a pair of x4 memory devices instead of one x8 memory device was a known option, as evidenced by Ellsberry's Figure 11, and would have been obvious to a person of ordinary skill in the art. *See* Pet. 68–73. Therefore, having considered the full record developed during the trial, we conclude that claims 3, 5, 12, and 16 are unpatentable as obvious over the combined teachings of Hiraishi, Butt, and Ellsberry.

F. Obviousness over Hiraishi, Butt, and Kim (Claims 8–10, 19, 20)

Petitioner asserts that claims 8–10, 19, and 20 would have been obvious over the combined teachings of Hiraishi, Butt, and Kim. Pet. 79–93. Apart from its arguments as to the independent claims, Patent Owner does not dispute Petitioner's contentions for these claims. *See* PO Resp. Below we summarize Petitioner's contentions and evidence, which we find persuasive.

These claims recite additional limitations relating to metastability conditions. Claim 8 recites,

> The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the

> module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

Petitioner argues that control device 400 in Hiraishi's Figure 7 receives a system clock signal and outputs a module clock signal and control signals (DRC signal) to the data buffers. Pet. 79–82 (citing Ex. 1005 ¶¶ 98, 99, 108, Figs. 6, 7; Ex. 1003 ¶¶ 235–238). Petitioner argues that DLL circuit 310 in the data buffer "generates the internal clock that is used to capture the DRC signal based on the received clock signal CK." Pet. 84 (citing Ex. 1003 ¶¶ 240–241). Petitioner argues that "the control information conveyed by the DRC signal may not be correctly captured if there is a metastability condition at the reception of the DRC" and, therefore, that a person of ordinary skill in the art "would have understood, and been motivated, to use the DLL circuit of Hiraishi to generate the internal clock from the received module clock signal CK with a specific phase relative to the DRC signals to avoid metastability." Pet. 84 (citing Ex. 1008, 1:21–31; Ex. 1003 ¶¶ 240–241). Petitioner argues that a person of ordinary skill in the art would have understood that metastability can happen in Hiraishi when the received clock and DRC signals are captured with an incorrect time alignment and that, "[i]n light of the possibility of erroneous DRC signal reading, it would have been obvious to" a person of ordinary skill in the art to "include the functionality of a known metastability condition detector (such as taught by Kim, EX1008)." Pet. 84–85 (citing Ex. 1003 ¶ 242). More particularly, Petitioner relies on Kim's disclosure of a

"metastability detection/prevention circuit." Pet. 85–86 (citing Ex. 1008, 1:21–31, 2:23–37. Kim discloses that "metastability detection/prevention circuit 20 preferably performs the function of detecting whether the output POUT of the main active circuit 10 has been disposed in a metastable state for a duration in excess of a transition duration." Ex. 1008, 2:32–37. Petitioner argues that a person of ordinary skill in the art would have been motivated to include metastability condition detector functionality, such as taught in Kim, to "obtain[] more reliable communications by avoiding metastability at the input of the clock and DRC signals, which signals carry important control information." Pet. 86 (citing Ex. 1005 ¶ 100; Ex. 1003 ¶ 244).

Claim 9 recites,

> The memory module of claim 8, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

Petitioner argues that a person of ordinary skill in the art would have understood that the phase of the received clock signal CK could be early or late relative to the phase of the received DRC signal, so she would have been motivated to generate both a delayed clock signal (in case the clock is early) and a delayed control signal DRC (in case the clock is late) and select the one which removes the metastability condition.

Pet. 87 (citing Ex. 1016 ¶¶ 18, 21–22, Fig. 3; Ex. 1030, Figs. 2A, 2B; Ex. 1028, Fig. 4; Ex. 1003 ¶¶ 245, 249–252); *see* Pet. 87–90 (setting forth detailed explanation for claim 9).

Claim 10 recites,

> The memory module of claim 9, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

Referring to its claim 9 contentions that delayed versions of both DRC (control) and clock signals would be generated, Petitioner argues that it would have been obvious to be able to select the delayed DRC signal if necessary, which would be indicated by a "second metastability indicator," and then capture (sample) the selected clock and control signals. Pet. 90–92 (citing Ex. 1016 ¶¶ 21–22, Fig. 3; Ex. 1028, 7:35–39, Fig. 4; Ex. 1008, code (57); Ex. 1030, Figs. 2A, 2B; Ex. 1003 ¶¶ 249–250, 257–262).

For claims 19 and 20, which recite method steps similar to the recited functionality of claims 8–10, Petitioner relies on its contentions for claims 8–10. Pet. 92–93.

As noted above, Patent Owner does not raise additional arguments for these claims. Petitioner's arguments and evidence, summarized above, are persuasive. Therefore, having considered the full record developed during

the trial, we conclude that claims 8–10, 19, and 20 are unpatentable as obvious over the combined teachings of Hiraishi, Butt, and Kim.

G. Remaining Grounds

Petitioner presents three additional grounds that apply certain teachings from Tokuhiro to the combinations discussed above to address a potential claim interpretation requiring that the "previous operation" (e.g., write) be in a different direction from the later operation (e.g., read). Pet. 93–127. Neither party proposes this interpretation in this proceeding, and we do not construe the claims to require this. Because we determine that all challenged claims are unpatentable as discussed above, we need not separately assess the patentability of the claims based on the grounds involving Tokuhiro. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d)."); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (nonprecedential) ("We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.").

H. Collateral Estoppel

After Petitioner filed its Reply, a panel of the Board issued a Final Written Decision in IPR2022-00236 ("236 FD"). Petitioner then sought leave to brief any impact that the 236 FD may have on this case. Ex. 3004. We did not authorize briefing, but we allowed the parties to address the issue during the oral hearing. Ex. 3004.

During the oral hearing, Petitioner argued that the 236 FD has collateral estoppel effect in this proceeding to resolve the disputed issues

against Patent Owner. *See* Tr. 10:5–18:13. As explained above, we conclude that the claims are unpatentable as obvious based on the record in this proceeding and, therefore, do not rely on collateral estoppel. We further note that the Court of Appeals for the Federal Circuit has "held that an IPR decision does not have collateral estoppel effect until that decision is affirmed or the parties waive their appeal rights." *United Therapeutics Corp. v. Liquidia Techs., Inc.*, 74 F.4th 1360, 1372 (Fed. Cir. 2023) (citing *XY, LLC v. Trans Ova Genetics, L.C.*, 890 F.3d 1282, 1294 (Fed. Cir. 2018) ("[A]n affirmance of an invalidity finding, whether from a district court or the Board, has a collateral estoppel effect on all pending or co-pending actions.")). No notice of appeal has been filed yet in IPR2022-00236, and the time for filing an appeal has not yet expired.

III. CONCLUSION[11]

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that claims 1–20 of the '506 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt	1, 2, 4, 6, 7, 11, 13–15, 17, 18	
3, 5, 12, 16	103(a)	Hiraishi, Butt, Ellsberry	3, 5, 12, 16	
8–10, 19, 20	103(a)	Hiraishi, Butt, Kim	8–10, 19, 20	
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt, Tokuhiro[12]		
3, 5, 12, 16	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry		
8–10, 19, 20	103(a)	Hiraishi, Butt, Tokuhiro, Kim		

[11] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[12] As explained above, because we determine that the challenged claims are unpatentable on other grounds, we decline to address the grounds involving Tokuhiro.

Overall Outcome			1–20	

IV. ORDER

Accordingly, it is

ORDERED that claims 1–20 of the '506 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 10,860,506 B2

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